IN THE CLAIMS

Please amend the claims as follows.

1. (Currently Amended) A digital processing integrated circuit to process media data, the integrated circuit including:

a data path arranged within the integrated circuit in a ring configuration to communicate the media data at different sampling rates synchronized with a sample-locked rate;

a plurality of processing modules positioned within the data path to process the media data;

a routing controller; and

a digital interface to communicate ~~communication~~ with a device external to the integrated circuit,

wherein the data path comprises a plurality of separate portions to communicate data between adjacent of the processing modules, ~~wherein~~ the separate portions of the data path to couple the adjacent processing modules in series to communicate the media data between the adjacent processing modules,

wherein the routing controller is configured to clock the media data ~~is clocked~~ in time-slots between the adjacent processing modules around the separate portions of the data path to provide communications from a source processing module to a target processing module,

wherein a number of the time-slots available for each of the different sampling rates is inversely related to each different sampling rate, and

~~wherein when the source and target processing modules are non-adjacent processing modules, the media data is clocked through one or more intervening processing modules~~

wherein each processing module is assigned a fixed output time-slot and a variable input time-slot.

2. (Currently Amended) The integrated circuit of claim 1, wherein the data path includes ~~defines a media data path including~~ a digital audio bus that interconnects the plurality of processing modules in series, ~~and~~

wherein data is communicated around the ring configuration in a single direction on the data path between adjacent processing modules,

wherein when the source and target processing modules are non-adjacent processing modules, the media data is clocked through one or more intervening processing modules,

wherein at least one of the processing modules comprises a sample rate converter module to convert digital audio data between two of the different sampling rates, and

wherein a differing number of the time-slots is used to communicate the digital audio data at the different sampling rates.

3. (Currently Amended) The integrated circuit of claim 1 [[2]], wherein ~~the digital audio bus communicates digital audio data in a plurality of time-slots, each particular processing module having at least one programmable or fixed time-slot from which data is received from the data path for processing by the particular processing module and wherein~~ media data corresponding to different processing modules is present at the same time on the data path.

4. (Currently Amended) The integrated circuit of claim 3 [[2]], wherein ~~the digital audio bus communicates digital audio data in a plurality of time-slots,~~ each ~~particular~~ processing module is ~~being~~ assigned at least one time-slot into which data processed by the particular processing module is exported to the digital audio bus and wherein data corresponding to different processing modules is present at the same time on the data path.

5. (Currently Amended) The integrated circuit of claim 3, wherein one of the processing modules is a Digital Signal Processor (DSP) and the data path communicates processing control data in ~~a plurality of~~ time-slots that are allocated to the processing modules under control of the DSP.

6. (Previously Presented) The integrated circuit of claim 1, wherein the separate portions of the data path comprise time division multiplexed buses to communicate a plurality of audio channels.

7. (Cancelled)

8. (Currently Amended) The integrated circuit of claim 1 [[7]], wherein the media data path includes a total number of time-slots for communicating media data at the ~~a plurality of~~ different sampling ~~bit~~ rates, and wherein the sum of a number of time-slots allocated to each of the different sampling ~~one of the plurality of bit~~ rates equals the total number of time-slots ~~summed across every bit rate~~.

9. (Previously Presented) The integrated circuit of claim 1, wherein each processing module is configured to:

selectively extract media data for processing from a first of the separate portions of the data path, the media data being provided in at least one time-slot of the first portion of the data path allocated to the processing module;

selectively insert processed media data into its allocated time-slot on a second of the separate portions for receipt by a next processing module; and

pass media data that it receives and that is associated with other processing modules unchanged along the second of the separate portions for receipt by the next processing module.

10. (Previously Presented) The integrated circuit of claim 1, wherein the number of processing modules connected along the data path is configurable, each processing module included in the device being allocated at least one time-slot provided by the data path.

11. (Previously Presented) The integrated circuit of claim 1, wherein the data path includes a control data path to communicate processing control data to at least one processing module, the processing control data being used by the processing module to process digital data received from the data path.

12. (Previously Presented) The integrated circuit of claim 11, wherein the processing control data includes parameters for digital signal processing by the processing module.

13. (Previously Presented) The integrated circuit of claim 12, wherein the parameters include at least one of filter parameters, time delay parameters, mixing parameters, or sample-rate conversion parameters.

14. (Previously Presented) The integrated circuit of claim 11, wherein the control data path is a time division multiplexed bus arranged to interconnect the plurality of modules in the ring configuration and wherein while the media data is communicated from the source processing module to the target processing module, any one or more of the processing modules can add media data to or receive media data from the media data path.

15. (Previously Presented) The integrated circuit of claim 11, wherein the processing control data includes streams of processing control data each of which is associated with a stream of media data communicated via the data path, each stream of processing control data being destined for an associated target processing module to which the stream of media data is communicated.

16. (Previously Presented) The integrated circuit of claim 15, wherein each stream of processing control data is arranged to be communicated via the control data path to arrive at its associated target module prior to a source processing module exporting the media data to the media data path.

17. (Previously Presented) The integrated circuit of claim 1, wherein the data path includes:

a plurality of media channels defined by time division multiplexed time-slots; and

a channel identification path including channel identification data to identify each media channel to the plurality of processing modules.

18. (Previously Presented) The integrated circuit of claim 17, wherein the data path includes a control data path to communicate processing control data to at least one processing module, the control data path including a plurality of control channels defined by time division

multiplexed time-slots, wherein the channel identification path identifies both the media channels and the control channels.

19. (Previously Presented) The integrated circuit of claim 1, wherein the data path includes a transport bus to communicate data between an external memory that is separate from the integrated circuit and at least one of the plurality of processing modules of the integrated circuit.

20. (Previously Presented) The integrated circuit of claim 1, wherein the plurality of processing modules are digital audio processing modules selected from the group consisting of an audio memory transport module, a digital delay line module, a sample rate converter module, a filter module, a mixer module, a DSP module, and a digital Input/Output module.

21. (Previously Presented) The integrated circuit of claim 1, wherein the integrated circuit is in a very large scale integration (VLSI) device.

22. (Currently Amended) A digital processing integrated circuit to process media data, the integrated circuit including:

a media data path arranged within the integrated circuit in a ring configuration to communicate the media data at different sampling rates synchronized with a sample-locked rate;

a plurality of processing modules positioned within the media data path and coupled in series to process the media data;

a processing control data path to communicate processing control data between the adjacent processing modules, wherein the processing control data defines processing functionality at an associated processing module and wherein each processing module of the plurality of processing modules is configured to communicate the media data and the processing control data to an adjacent processing module;

the integrated circuit including a routing controller to route the media data and the processing control data along the data path to an associated processing module; and

a digital interface to communicate media data with a device external to the integrated circuit,

wherein the media data is clocked by the routing controller in time-slots between adjacent processing modules around separate portions of the data path to provide communications from a ~~the~~ source processing module to a ~~the~~ target processing module,

wherein a number of the time-slots available for each of the different sampling rates is inversely related to each different sampling rate, and

~~wherein when the source and target processing modules are non-adjacent processing modules, the media data is clocked through one or more intervening processing modules~~

wherein each processing module is assigned a fixed output time-slot and a variable input time-slot.

23. (Currently Amended) The integrated circuit of claim 22, wherein ~~while the media data is communicated from the source processing module to the target processing module, any one or more of the processing modules can add media data to or receive media data from the media data path~~ at least one of the processing modules comprises a sample rate converter module to convert digital audio data between two of the different sampling rates, and

wherein a differing number of the time-slots is used to communicate the digital audio data at the different sampling rates.

24. (Currently Amended) A method to process media data in a plurality of processing modules in a digital media processing integrated circuit, the method including:

communicating, at each processing module within the integrated circuit, the media data from the processing module to an adjacent processing module along a data path interconnecting the plurality of processing modules in a ring configuration until media data from a source processing module is received at a target processing module of the plurality of processing modules, the media data being communicated at different sampling rates synchronized with a sample-locked rate; and

communicating media data between the data path and a device external to the integrated circuit,

wherein the processing modules are positioned within the data path and coupled in series,

wherein the media data is clocked in time-slots between adjacent processing modules around separate portions of the data path to provide communications from the source processing module to the target processing module,

wherein a number of the time-slots available for each of the different sampling rates is inversely related to each different sampling rate, and

wherein each processing module is assigned a fixed output time-slot and a variable input time-slot.

~~wherein when the source and target processing modules are non-adjacent processing modules, the media data is clocked through one or more intervening processing modules.~~

25. (Currently Amended) The method of claim 24, which includes communicating the media data sequentially between the plurality of processing modules,

wherein at least one of the processing modules comprises a sample rate converter module to convert digital audio data between two of the different sampling rates, and

wherein a differing number of the time-slots is used to communicate the digital audio data at the different sampling rates.

26. (Currently Amended) The method of claim 24, wherein the data path includes a processing module identifier that identifies the source processing module that provides the media to the data path, and

wherein when the source and target processing modules are non-adjacent processing modules, the media data is clocked through one or more intervening processing modules.

27. (Previously Presented) The method of claim 24, last processing module of the plurality of processing modules is communicated to first processing module of the plurality of processing modules.

28. (Currently Amended) The method of claim 24, wherein ~~the data path includes a plurality of time-slots,~~ the method includes ~~including~~ providing the processed media data into a

time-slot associated with a source processing module and wherein data corresponding to different processing modules is present at the same time on the data path.

29. (Original) The method of claim 24, wherein the data path includes a digital media path and a processing control path, the method including:

providing the media data in the form of audio data to the digital media path; and

providing processing control data to the processing control data path, the processing control data controlling the processing of the audio data by the target processing module.

30. (Currently Amended) The method of claim 24, ~~which includes providing the media data in at least one time-slot of a digital audio bus defined by the data path, each particular processing module having at least one programmable or~~ wherein during the assigned fixed output time-slot, each processing is configured to output ~~from which~~ data ~~is received from~~ to the digital audio bus, and

wherein during the assigned variable input time-slot, each processing module is configured to receive data from the digital audio bus for processing by the particular processing module.

31. (Cancelled)

32. (Currently Amended) The method of claim 24 [[31]], wherein one of the processing modules is a Digital Signal Processor (DSP), the method including communicating processing control data via the data path in ~~a plurality of~~ time-slots that are allocated to the processing modules under control of the DSP.

33. (Original) The method of claim 24, wherein the data path is time division multiplexed bus including a plurality of audio channels.

34. (Currently Amended) The method of claim 33, which includes communicating data between the plurality of processing modules at the different sampling ~~bit~~ rates ~~that differ~~.

35. (Currently Amended) The method of claim 34 [[32]], wherein the data path includes a total number of time-slots for communicating media data at the different sampling ~~a plurality of different bit~~ rates, the method including allocating a number of time-slots to each one of the different sampling ~~plurality of bit~~ rates so that a sum of the number of slots allocated ~~to the plurality of bit rates~~ equals the total number of time-slots ~~summed across every bit rate~~.

36. (Previously Presented) The method of claim 24, wherein the number of processing modules connected in series by the data path is configurable, the method including allocating at least one time-slot provided by the data path to each processing module to allow data corresponding to different processing modules to be present at the same time on the data path.

37. (Original) The method of claim 24, which includes communicating processing control data to at least one target processing module via a control data path, the processing control data being used by the target processing module to process digital data received from a media data path.

38. (Original) The method of claim 37, which includes processing the media data using the processing control data that includes parameters for digital signal processing.

39. (Previously Presented) The method of claim 38, which includes communicating parameters including at least one of filter parameters, time delay parameters, mixing parameters, or sample-rate conversion parameters to a processing module via the control data path.

40. (Original) The method of claim 37, which includes communicating the processing control data in a time division multiplexed fashion.

41. (Original) The method of claim 37, wherein the processing control data includes streams of processing control data each of which is associated with a stream of media data

communicated via the media data path, each stream of processing control data being destined for an associated target processing module to which the stream of media data is communicated.

42. (Original) The method of claim 41, which includes communicating each stream of processing control data via the control data path to arrive at its target processing module prior to exporting the media data from its source processing module to the media data path.

43. (Previously Presented) The method of claim 24, wherein the data path includes:

a plurality of media channels defined by time division multiplexed time-slots; and

a channel identification path including channel identification data to identify each media channel to the plurality of processing modules.

44. (Original) The method of claim 43, which includes communicating processing control data to at least one target processing module via a control data path, the control data path including a plurality of control channels defined by time division multiplexed time-slots, wherein the channel identification path identifies both the media channels and the control channels.

45. (Previously Presented) The method of claim 24, which includes communicating data between an external memory that is separate from the integrated circuit and at least one of the plurality of processor modules via a transport bus of the integrated circuit.

46. (Original) The method of claim 24, which includes communicating media data between digital audio processing modules selected from the group consisting of an audio memory transport module, a digital delay line module, a sample rate converter module, a filter module, a mixer module, a DSP module, and a digital Input/Output module.

47. (Currently Amended) A computer-readable that stores ~~machine-readable medium embodying~~ a sequence of instructions for execution by one or more processors to perform the following operations ~~that, when executed by the machine, cause the machine~~ to process media

data in a plurality of processing modules by configuring the processing modules ~~in a digital media processing integrated circuit, the instructions being~~ to:

communicate, at each processing module within the integrated circuit, the media data from the processing module to an adjacent processing module along a data path interconnecting the plurality of processing modules in a ring configuration until media data from a source processing module is received at a target processing module of the plurality of processing modules, the media data being communicated at different sampling rates synchronized with a sample-locked rate; and

communicate media data between the data path and a device external to the integrated circuit via a digital interface,

wherein the processing modules are positioned within the data path and coupled in series,

wherein the media data is clocked between adjacent processing modules around separate portions of the data path to provide communications from the source processing module to the target processing module, wherein a number of the time-slots available for each of the different sampling rates is inversely related to each different sampling rate, and

wherein each processing module is assigned a fixed output time-slot and a variable input time-slot.

~~wherein when the source and target processing modules are non-adjacent processing modules, the media data is clocked through one or more intervening processing modules.~~

48. (Currently Amended) The computer-readable ~~machine-readable~~ medium of claim 47, wherein the media data is communicated sequentially between the plurality of processing modules,

wherein at least one of the processing modules comprises a sample rate converter module to convert digital audio data between two of the different sampling rates, and

wherein a differing number of the time slots is used to communicate the digital audio data at the different sampling rates. .

49. (Currently Amended) The computer-readable ~~machine-readable~~ medium of claim 47, wherein the data path includes a processing module identifier that identifies the source processing module that provides the media to the data path.

50. (Currently Amended) The computer-readable ~~machine-readable~~ medium of claim 47, wherein media data received at a last processing module of the plurality of processing modules is communicated to first processing module of the plurality of processing modules.

51. (Currently Amended) The computer-readable ~~machine-readable~~ medium of claim 47, wherein ~~the data path includes a plurality of time-slots and~~ the processed media data is provided in a time-slot associated with a source processing module and wherein data corresponding to different processing modules is present at the same time on the data path.

52. (Currently Amended) The computer-readable ~~machine-readable~~ medium of claim 47, wherein the data path includes a digital media path and a processing control path, the instructions being to:

provide the media data in the form of audio data to the digital media path; and

provide processing control data to the processing control data path, the processing control data controlling the processing of the audio data by the target processing module.

53. (Cancelled)

54. (Currently Amended) The computer-readable ~~machine-readable~~ medium of claim 47, wherein each particular processing module is assigned at least one programmable or fixed time-slot of a digital audio bus defined by the data path, and wherein digital audio data processed by the particular processing module is exported to the programmable or fixed time-slot.

55. (Currently Amended) The computer-readable ~~machine-readable~~ medium of claim 54, wherein one of the processing modules is a Digital Signal Processor (DSP), and wherein

processing control data is communicated via the data path in the ~~a plurality of~~ time-slots that are allocated to the processing modules under control of the DSP.

56. (Currently Amended) The computer-readable ~~machine-readable~~ medium of claim 47, wherein the data path is a time division multiplexed bus including a plurality of audio channels.

57. (Currently Amended) The computer-readable ~~machine-readable~~ medium of claim 56, wherein data is communicated between the plurality of processing modules at the different sampling rates ~~bit rates that differ~~.

58. (Currently Amended) The computer-readable ~~machine-readable~~ medium of claim 55, wherein the data path includes a total number of time-slots for communicating media data at ~~a plurality of~~ the different ~~bit~~ sampling rates, and wherein a number of time-slots are allocated to each ~~one~~ of the different sampling ~~plurality of bit~~ rates so that a sum of the number of time-slots allocated to each ~~one~~ of the different sampling ~~plurality of bit~~ rates equals the total number of time-slots ~~summed across every bit rate~~.

59. (Currently Amended) The computer-readable ~~machine-readable~~ medium of claim 47, wherein the number of processing modules connected in series by the data path is configurable and wherein at least one time-slot is provided by the data path to each processing module to allow data corresponding to different processing modules to be present at the same time on the data path.

60. (Currently Amended) The computer-readable ~~machine-readable~~ medium of claim 47, wherein processing control data is communicated to at least one target processing module via a control data path, the processing control data being used by the target processing module to process digital data received from a media data path.

61. (Currently Amended) The computer-readable ~~machine-readable~~ medium of claim 60, wherein the media data is processed using the processing control data that includes parameters for digital signal processing.

62. (Currently Amended) The computer-readable ~~machine-readable~~ medium of claim 61, wherein parameters including at least one of filter parameters, time delay parameters, mixing parameters, and sample rate conversion parameters are communicated to a processing module via the control data path.

63. (Canceled)

64. (Currently Amended) The computer-readable ~~machine-readable~~ medium of claim 60, wherein the processing control data includes streams of processing control data each of which is associated with a stream of media data communicated via the media data path, each stream of processing control data being destined for an associated target processing module to which the stream of media data is communicated.

65. (Currently Amended) The computer-readable ~~machine-readable~~ medium of claim 64, which includes communicating each thread of processing control data via the control data path to arrive at its target processing module prior to exporting the media data from its source processing module to the media data path.

66. (Currently Amended) The computer-readable ~~machine-readable~~ medium of claim 47, wherein the data path includes:

a plurality of media channels defined by time division multiplexed time-slots; and

a channel identification path including channel identification data to identify each media channel to the plurality of processing modules.

67. (Currently Amended) The computer-readable ~~machine-readable~~ medium of claim 66, wherein processing control data is communicated to at least one target processing module via a

control data path, the control data path including a plurality of control channels defined by time division multiplexed time-slots, wherein the channel identification path identifies both the media channels and the control channels.

68. (Currently Amended) The computer-readable ~~machine-readable~~ medium of claim 47, wherein data is communicated between an external memory and at least one of the plurality of processor modules via a transport bus.

69. (Currently Amended) The computer-readable ~~machine-readable~~ medium of claim 47, media data is communicated between digital audio processing modules selected from the group consisting of an audio memory transport module, a digital delay line module, a sample rate converter module, a filter module, a mixer module, a DSP module, and a digital Input/Output module.

70. (Currently Amended) The integrated circuit of claim 1, wherein each processing module includes an input to receive data in a first time-slot sent by a first adjacent processing module over a first of the separate portions, and an output to send data in a second time-slot to a second adjacent processing module over a second of the separate portions to allow serial interconnection of the processing modules in the ring configuration.

71. (Previously Presented) The integrated circuit of claim 70, wherein the input includes at least one input register connected by the data path to the first adjacent processing module, and the output includes at least one output register connected by the data path to the second adjacent processing module and media data is clocked along the data path by the at least one input register and the at least one output register.